STIC Search Report
EIC 2100

STIC Database Tracking Number: 166795

TO: Gregory Hein
Location: RND2c55
Art Unit: 188
Monday, September 26, 2005

Case Serial Number: 10/636042

From: Emory Damron
Location: EIC 2100
RND 4B19
Phone: 571-272-3520

Emory.Damron@uspto.gov

Search Notes

Dear Gregory,

Please find below your fast and focused search.
References of potential pertinence have been tagged, but please review all the packets in case you like something I didn't.
Of those references which have been tagged, please note any manual highlighting which I've done within the document.
In addition to searching on Dialog, I also searched EPO/JPO/Derwent.
There may be a few decent references contained herein, but I'll let you determine how useful they may be to you.
Please contact me if I can refocus or expand any aspect of this case, and please take a moment to provide any feedback (on the form provided) so EIC 2100 may better serve your needs. Good Luck!

Sincerely,
Emory Damron
Technical Information Specialist
EIC 2100, US Patent & Trademark Office
Phone: (571) 272-3520
Emory.damron@uspto.gov

STIC EIC 2100 Search Request Form

166795

119

Today's Date: 9/25/2005

What date would you like to use to limit the search?

Priority Date: 8/7/2003 Other:

Name Gregory Hein

AU 2188 Examiner # 81604

Room # 2C55 Phone x-4180

Serial # 10/686042

Format for Search Results (Circle One):

PAPER DISK EMAIL

Where have you searched so far?

USP DWPI EPO JPO ACM IBM TDB

IEEE INSPEC SPI Other _____

Is this a "Fast & Focused" Search Request? (Circle One) YES NO

A "Fast & Focused" Search is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2100 and on the EIC2100 NPL Web Page at http://ptoweb/patents/stic/stic-tc2100.htm.

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

On the included sheet, claim 1. The process described here is called "extended remote copy". The copy manager or storage mover or data mover, which are equivalent names, stores data from multiple sources in an intermingled fashion. It also creates a log of the data stored. These are the aspects I can't find. The intermingling of multi-threaded data and the creation of a log. It doesn't have to be retrieval. Any system writing or reading using this method is great.

Keywords: Extended Remote Copy, Data Mover, Copy Manager, Sequential, Intermingle, Mix(ed) Data, Interleave, magnetic storage, magnetic device, multi-thread, multi-source, multiple source.

7/11/11

STIC Searcher Emory Dameron Phone 2-3520

Date picked up 9/26/05 Date Completed 9/26/05

Search and Information Resources Administration

xCopy

STIC Search Results Feedback Form

EIC 2100

Questions about the scope or the results of the search? Contact ***the EIC searcher or contact:***

Anne Hendrickson, EIC 2100 Team Leader
272-3490, RND 4B28

Voluntary Results Feedback Form

➢ *I am an examiner in Workgroup:* 2188 *Example: 2133*

➢ *Relevant prior art **found**, search results used as follows:*

- ☐ 102 rejection
- ☐ 103 rejection
- ☐ Cited as being of interest.
- ☐ Helped examiner better understand the invention.
- ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature
  (journal articles, conference proceedings, new product announcements etc.)

➢ *Relevant prior art **not found:***

- ☐ Results verified the lack of relevant prior art (helped determine patentability).
- ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2100 RND, 4B28

```
Set     Items   Description
S1       7870   (EXTEND? OR EXTRA? OR REDUND? OR SECOND? OR 2ND OR BACKUP?
           OR BACK?()UP)(2N)(REMOTE? OR OFFSITE? OR DISTAL? OR DISTANT? -
           OR GLOBAL? OR ("NOT" OR NON)()LOCAL? OR OFF()SITE)
S2    4108356   COPY? OR STORE? OR STORAGE? OR WRITE? OR WRITING?
S3    1942025   RECORD? OR MEMOR? OR BACKUP? OR BACK?()UP
S4     268430   (MAGNETIC OR MEMOR?)(2N)(STORAG? OR TAPE? OR DEVIC? OR DIS-
           K? OR DISC?)
S5     813110   CONTROLLER? OR MANAGER? OR SUPERVISOR? OR AUTHORIT?
S6       2213   (STORAG? OR DATA?)()(MOVER? OR ROUTER? OR MULTIPLEX? OR MU-
           X?)
S7    2415989   MULTIP? OR MULTIT? OR PLURAL? OR MANY? OR SEVERAL? OR ARRA-
           Y? OR MULTITHREAD? OR MULTI()THREAD?
S8    5051005   DATA? OR PACKET? OR INPUT? OR THREAD? OR INFORMATION? OR I-
           NFO? OR FILE? OR SOURC?
S9      24846   INTERMINGL? OR INTERMIX? OR INTERLEAV? OR COALESC?
S10     24846   INTERMINGL? OR INTERMIX? OR INTERLEAV? OR COALESC?
S11    603149   COMMINGL? OR COMMIX? OR INTEGRAT? OR INTERLAC? OR SHUFFL? -
           OR INTERWEAV?
S12    250867   CHRONICL? OR ARCHIV? OR LOG OR LOGS OR LOGGED OR LOGGING? -
           OR INDEX?
S13   1083657   HISTOR? OR TRACK? OR LIBRAR? OR RECORD? ? OR DIARY? OR REG-
           IST? OR LIST? ?
S14    587390   MONITOR? OR WATCH? OR AUDIT? OR ACCOUNT?
S15   5863670   LOCATION? OR ADDRESS? OR SITE? ? OR LOCALE? OR POSITION? OR
            SECTOR? OR LOCUS? OR SECTION? OR SEQUEN? OR IDENTIF?
S16   1242704   IC=G06F?
S17    186751   S7(7N)S8 AND S2:S4
S18        80   S17 AND S1
S19     10241   S17 AND S9:S11
S20      1130   S19 AND S5:S6
S21       195   S20 AND S12:S14 AND S15
S22    997622   S20 AND S9:S11(7N)S8 AND S2:S4(7N)S8 OR (S2:S4 OR S8)(7N)S-
           15
S23       173   S20 AND S9:S11(7N)S8 AND S2:S4(7N)S8 AND (S2:S4 OR S8)(7N)-
           S15
S24         7   S18 AND S9:S11
S25        64   S21 AND S23
S26        71   S24:S25
S27    193287   PR=2004:2005
S28        68   S26 NOT S27
S29        68   IDPAT (sorted in duplicate/non-duplicate order)
S30       304   S21 OR S23
S31       242   S30 NOT S28
S32        48   S31 NOT INTEGRAT?
S33        47   S32 NOT S27
S34        47   IDPAT (sorted in duplicate/non-duplicate order)
File 347:JAPIO Nov 1976-2005/Apr(Updated 050801)
         (c) 2005 JPO & JAPIO
File 350:Derwent WPIX 1963-2005/UD,UM &UP=200561
         (c) 2005  Thomson Derwent
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29/3,K/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015765173 **Image available**
WPI Acc No: 2003-827375/200377
Method for operating interleaver memory
Patent Assignee: ELECTRONICS & TELECOM RES INST (ELTE-N); KOREA ELECTRONICS & TELECOM RES INST (KOEL-N)
Inventor: JUNG H B; KIM G S; LEE S H; LIM I G; CHUNG H B
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
KR 2003056566	A	20030704	KR 200186828	A	20011228	200377 B
KR 431082	B	20040512	KR 200186828	A	20011228	200459

Priority Applications (No Type Date): KR 200186828 A 20011228
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2003056566	A		1	H04B-001/69	
KR 431082	B			H04B-001/69	Previous Publ. patent KR 2003056566

Method for operating interleaver memory

Abstract (Basic):
... A method for operating an **interleaver memory** is provided to divide a **memory** area of one **interleaver memory** into **several** banks, and to **store** channel **data** in blank banks, so as to improve **memory** use efficiency when a plurality of subscribers access a base station.
... If a **writing** operation is requested(1), a micro **controller** (10) decides a sub modulator and a modulator unit(140)(2), and reads a bank state **register** of a bank **controller** (120) to recognize **locations** and sizes of blank banks(3). The micro **controller** (10) calculates the number of consecutive blank banks and a bank of a minimum start **address** (4), and **writes data** in a bank allocation **register** (5). The bank state **register** of the bank **controller** is set(51). The micro **controller** (10) respectively **stores** calculated values in a frame offset **register** , an **address** offset **register** and a spreading factor value **register** of the modulator unit(140)(6). The micro **controller** (10) receives channel **data** for **interleaving** and **sequentially writes** the channel **data** in the blank banks of an **interleaver memory** (7). A frame **controller** of the modulator unit(140) generates a frame synchronous signal(61). If the frame synchronous signal is 1(one)(62), a **memory** read **address** and control signal generator of the modulator unit(140) generates a read **address** , a **memory** selection signal and a read signal(63), and produces a signal for reading the channel **data**, **stored** in the **interleaver memory** by referring to the values **stored** in the **registers** (64). The channel **data** are read and provided to each modulator unit(140), then modulated(65). If the channel **data stored** in the **interleaver memory** are completely read, the **memory** read **address** and control signal generator generates a flag signal to notify the completion of **interleaving** (66...
...Title Terms: **INTERLEAVED** ;

29/3,K/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015644979 **Image available**
WPI Acc No: 2003-707162/200367
XRPX Acc No: N03-564880
Cache data mirroring method for redundant array of independent disks system, involves copying data **from main controller to alternate** controller **which** writes data **to** storage **system when failure of main** controller **is detected**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: OTTERNESS N S; SKAZINSKI J G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6574709	B1	20030603	US 99410168	A	19990930	200367	B

Priority Applications (No Type Date): US 99410168 A 19990930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6574709	B1		27	G06F-011/00	

Cache data mirroring method for redundant array of independent disks system, involves copying data **from main controller to alternate** controller **which** writes data **to** storage **system when failure of main** controller **is detected**

Abstract (Basic):
... A main **controller** (17) **stores** relevant **data** to be written in a **storage** system (50), in response to a request from a computer (5). The **stored data** are cached and copied to an alternate **controller** where status of cache **data** is maintained by mirror valid flags, **sequences** and maps. The **data** are then written in the **storage** system from the alternate **controller** , when failure of the main **controller** is detected.
... 2) method for **tracking** mirrored data...

...3) main **controller** ; and...

...4) method for operating main and alternate **storage controllers** .
...

...For mirroring cache **data** to **data storage** system such as redundant **array** of independent disks (RAID) system including disk drives, tape drives, printers, compact **disk** -read only **memory** (CD-ROM) drives, scanners and optical disks, used with computer systems in server environments and multi- **controller** environments...

...Since data in the main and alternate **controllers** are linked explicitly, the need for performing queries and waiting for reply from **memories** is made unnecessary. Number of cache mirroring operations are reduced by **coalescing multiple data** mirror operations into single mirroring operation...

... **controller** (17...

...random access **memory** (40...

... **data storage** system (50

...Title Terms: **COPY ;**

29/3,K/18 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013314932 **Image available**
WPI Acc No: 2000-486869/200043
XRPX Acc No: N00-362272
Interleave **releasing apparatus for digital** data **broadcasting**, stores **shifted** position **of initial** data , **and function value generator generates new function value for** data interleaving **point and** register
Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000183757	A	20000630	JP 98356807	A	19981215	200043	B

Priority Applications (No Type Date): JP 98356807 A 19981215
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000183757	A		12	H03M-013/27	

Interleave **releasing apparatus for digital** data **broadcasting**, stores **shifted** position **of initial** data , **and function value generator generates new function value for** data interleaving **point and** register

Abstract (Basic):
... **Address**s generator (10) has initial value generator (101) which **stores** shifted **position** of initial **data** , function value generator (102) to generate new function value from initial value or old function value based on **data interleaving** point. A **register stores** either of the values chosen by selector (103). A **controller** (105) **stores** destination of **data** segment in lead **data** unit after **interleaving** .
... For orthogonal frequency division **multiplex** (OFDM) digital **data** broadcasting...

...The **interleave** releasing apparatus is inexpensive because random access **memory** is not required for storing **interleave** rule as the **interleave** point is generated by function value generator. High speed **interleaving** is performed since clock frequency is high and also function value generator is parallely connected...

...The figure shows the block diagram of **interleave** release apparatus...

... **Address** generator (10
Title Terms: **INTERLEAVED** ;

29/3,K/20 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012543561 **Image available**
WPI Acc No: 1999-349667/199930
XRPX Acc No: N99-261516
Financial transaction processing system for transmission of financial information over internet
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: BENNETT W E; BOEHME R F; KALLNER S; LEVY S E; MATCHEN P M; RYAN M J; THOMPSON R D
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2332604	A	19990623	GB 9819159	A	19980902	199930	B
JP 11250146	A	19990917	JP 98325132	A	19981116	199949	
US 6092121	A	20000718	US 97993232	A	19971218	200037	
GB 2332604	B	20030319	GB 9819159	A	19980902	200321	
TW 495680	A	20020721	TW 98116068	A	19980928	200329	

Priority Applications (No Type Date): US 97993232 A 19971218
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2332604	A		32	H04L-012/46	
JP 11250146	A		12	G06F-017/60	
US 6092121	A			G06F-015/16	
GB 2332604	B			H04L-012/46	
TW 495680	A			G06F-017/00	

Abstract (Basic):
... The system electronically **integrates** data captured in heterogeneous information systems, and transmits that **data** reliably and securely over Internet, between **multiple** diverse servers, to a system for electronically transferring data to heterogeneous information systems. The data...
... A **store** and forward mechanism (39) receives and queues client objects for transmission to remote servers (40...

...from the data contained in the client object. A map server function running on a **remote** computer system **extracts** the data buffer and invokes an appropriate message handler. The remote computer system receives data...

... **Store** and forward mechanism (39
? pause
?
PLEASE ENTER A COMMAND OR BE LOGGED OFF IN 5 MINUTES
?

29/3,K/23 (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011915703 **Image available**
WPI Acc No: 1998-332613/199829
XRPX Acc No: N98-259633
Intelligent distributed data transfer apparatus - includes series of finite state machines each with programmable logic array for receiving down-loading of control programs and state register **for storing state of FSM which receive control signals from** integrated **distribution control**
Patent Assignee: IND TECHNOLOGY RES INST (INTE-N)
Inventor: HSIEH H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5761200	A	19980602	US 93147322	A	19931027	199829 B

Priority Applications (No Type Date): US 93147322 A 19931027
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5761200	A		17	G06F-013/00	

... **machines each with programmable logic array for receiving down-loading of control programs and state** register **for storing state of FSM which receive control signals from** integrated **distribution control**

...Abstract (Basic): system includes a number of distributed data transfer units for connection to processing units. A **integrated** distribution **controller** is connected to the **data** transfer units for **monitoring** and controlling timing and **sequence** of transferring **data** in each of the **data** transfer units so the data transfer units transfer the data in divisible portions over a...

...include a series of data bus branches and a bus trunk which connects between an **integrated storage** device and the **integrated** distribution control. The **data** bus branches connect between the **integrated** distribution control and the processing units. The **integrated** distribution control controls and coordinates the timing and **sequence** of **data** transfer from the bus trunk to each of the bus branches. A programmable control, within the **integrated** distribution **controller** , downloads control programs for changing schemes for controlling the timing of a **sequence** of **data** transfer. The programmable control includes finite state machines (FSMs), for each of the **data** bus branches, with a programable logic **array** for receiving the downloading of control programs and a state **register** for storing a state of the FSMs. Each of the FSMs receives a control signal from the **integrated** distribution control...

...USE - For transferring **data** among **several** processing units and **integrated data storage** device...
...Title Terms: **REGISTER** ;

29/3,K/27 (Item 27 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010742680 **Image available**
WPI Acc No: 1996-239635/199624
XRPX Acc No: N96-200531
Information **processing circuit for accessing interleaved** storage **modules - has multiple bus mastering devices and** multiple interleaved memory **modules combined to form** information **processing circuit**
Patent Assignee: AST RES INC (ASTR-N); SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: BENNETT B R
Number of Countries: 023 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9613774	A1	19960509	WO 95US10835	A	19950825	199624	B
AU 9534158	A	19960523	AU 9534158	A	19950825	199635	
US 5590299	A	19961231	US 94331290	A	19941028	199707	
AU 687627	B	19980226	AU 9534158	A	19950825	199821	
CA 2203900	C	20000606	CA 2203900	A	19950825	200041	
			WO 95US10835	A	19950825		

Priority Applications (No Type Date): US 94331290 A 19941028
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9613774	A1		29	G06F-012/00	
Designated States (National): AU CA CN JP KR MX					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
AU 9534158	A			G06F-012/00	Based on patent WO 9613774
US 5590299	A		17	G06F-012/00	
AU 687627	B			G06F-012/00	Previous Publ. patent AU 9534158 Based on patent WO 9613774
CA 2203900	C	E		G06F-013/42	Based on patent WO 9613774

Information **processing circuit for accessing interleaved** storage **modules**...

...**has multiple bus mastering devices and** multiple interleaved memory **modules combined to form** information **processing circuit**

...Abstract (Basic): The circuit includes a system bus, a first and second **interleaved memory** modules and first and second central processing unit (CPU) modules in communication with the **interleaved memory** modules via the system bus...

...Each of the modules comprises a CPU and a cache **memory** , an **address** decoder circuit, an **address** latch circuit, an **address** comparator circuit, an **interleave register** , control circuitry and a bus **controller** . The bus **controller** receives signals generated by the control circuitry to cause the CPU module to retain control...
...Abstract (Equivalent): An **information** processing system including **multiple** bus mastering modules, said system comprising...

...a plurality of **memory** modules in communication with said system bus; and...

...mastering modules, wherein each of said bus mastering modules includes a subcircuit which, before an **address** directed to one of said **memory** modules is placed on said system bus, **monitors** said **address**

requested by said bus mastering modules, and wherein said subcircuit grants the local bus mastering circuit control of the system bus for a next **data** transfer cycle if a current **memory address** is to a different **memory** module than a previous **address** request...

...Title Terms: **INTERLEAVED** ;

29/3,K/30 (Item 30 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010410571 **Image available**
WPI Acc No: 1995-311885/199541
Related WPI Acc No: 1995-256344
XRPX Acc No: N95-235653
Magnetic disk data storage **device with spiral** tracks **- has spiral patterns on opposite surfaces of disk spiralling in opposite directions and reads one surface as actuator sweeps in and other surface as actuator sweeps out**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC); HITACHI GLOBAL STORAGE TECHNOLOGIES NETH (HITA-N)
Inventor: BROWN D H; CUNNINGHAM E A; GREENBERG R; OTTESEN H H; SMITH G J; VANLEEUWEN G W; BILLINGS R A; CUNNINGHAM B A; VAN LEEUWEN G W
Number of Countries: 010 Number of Patents: 017
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
CA 2138301	A	19950722	CA 2138301	A	19941215	199541	B
EP 701246	A2	19960313	EP 95480084	A	19950713	199615	
JP 8063898	A	19960308	JP 95127677	A	19950526	199620	
TW 270193	A	19960211	TW 94111744	A	19941215	199621	
BR 9503412	A	19960521	BR 953412	A	19950724	199626	
EP 701246	A3	19960605	EP 95480084	A	19950713	199632	
US 5594924	A	19970114	US 94184417	A	19940121	199709	
			US 94288525	A	19940810		
			US 95443838	A	19950518		
US 5619387	A	19970408	US 94184417	A	19940121	199720	
			US 94288525	A	19940810		
			US 95444175	A	19950518		
			US 96689582	A	19960812		
US 5630104	A	19970513	US 94184417	A	19940121	199725	
			US 94288525	A	19940810		
			US 95444116	A	19950518		
CN 1128386	A	19960807	CN 95104772	A	19950425	199750	
CA 2138301	C	19981215	CA 2138301	A	19941215	199909	
KR 218611	B1	19990901	KR 9524501	A	19950809	200104	
JP 2002140864	A	20020517	JP 95127677	A	19950526	200237	
			JP 2001215689	A	19950526		
CN 1359070	A	20020717	CN 95104772	A	19950425	200268	
			CN 2001124475	A	19950425		
JP 3532296	B2	20040531	JP 95127677	A	19950526	200436	
CN 1077308	C	20020102	CN 95104772	A	19950425	200513	
JP 3660612	B2	20050615	JP 95127677	A	19950526	200544	
			JP 2001215689	A	20010716		

Priority Applications (No Type Date): US 94288525 A 19940810; US 94184417 A 19940121; US 95443838 A 19950518; US 95444175 A 19950518; US 96689582 A 19960812; US 95444116 A 19950518
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
CA 2138301	A		54	G11B-007/09	
EP 701246	A2	E	24	G11B-005/012	
Designated States (Regional): DE FR GB					
JP 8063898	A		22	G11B-020/12	
TW 270193	A			G06K-001/00	
BR 9503412	A			G11B-019/20	
EP 701246	A3			G11B-007/09	
US 5594924	A		21	G06F-009/312	CIP of application US 94184417
					Div ex application US 94288525
US 5619387	A		21	G11B-005/55	CIP of application US 94184417

				Div ex application US 94288525 Cont of application US 95444175
US 5630104	A	21	G06F-017/00	CIP of application US 94184417 Div ex application US 94288525
CN 1128386	A		G11B-005/00	
CA 2138301	C		G11B-020/12	
KR 218611	B1		G11B-007/26	
JP 2002140864	A	21	G11B-020/10	Div ex application JP 95127677
CN 1359070	A		G06F-012/06	Div ex application CN 95104772
JP 3532296	B2	20	G11B-020/12	Previous Publ. patent JP 8063898
CN 1077308	C		G11B-005/00	
JP 3660612	B2	24	G11B-020/10	Div ex application JP 95127677 Previous Publ. patent JP 2002140864

Magnetic disk data storage **device with spiral** tracks -

...Abstract (Basic): The device comprises a first and a second magnetic **recording** surface located on a disk rotatably mounted on a spindle, and having an inner and an outer edge. A spindle motor rotates the disk in the predetermined direction. The first **recording** surface is formatted to contain a spiral **data track** spiralling inward from the outer edge. The second **recording** surface is formatted to contain a **data track** spiralling outward from the inner edge toward the outer edge of the disk...

...movable actuator on each side of the disk for accessing data by following the spiral **tracks** . The patterns of the **tracks** on the two surfaces spiral in opposite direction. The **data stored** on the disk is pref. multimedia **data** which does not require a very low error rate ...

...USE/ADVANTAGE - Esp. **storage** of multimedia **data** , e.g. in video-on-demand applications. Provides more efficient **storage** of large amount of multimedia **data** at reduced cost and at more suitable access speed...

...Abstract (Equivalent): A method for providing multimedia presentation **data** , said multimedia presentation being divisible into a **plurality** of portions corresponding to successive time intervals, each said portion being for presentation during the...

...reading a **plurality** of multimedia **data** segments from at least one mass **storage** device, each of said multimedia **data** segments containing multimedia data from a respective one of said portions...

...wherein a **plurality** of multimedia **data** segments contain **data** from each said portion, and wherein successive data segments read during said step of reading a **plurality** of multimedia **data** segments contain **data** from different ones of said **plurality** of portions, the **data** segments containing **data** from a particular one of said **plurality** of portions being **interleaved** among **data** segments containing **data** from other portions...

...selectively transferring each of said multimedia **data** segments to a selected one of a **plurality** of buffers, wherein each of said plurality of buffers corresponds to a respective one of...

...A rotating disk **data storage** device, comprising...

...disk rotatably mounted on a spindle, said at least one disk having a first annular **recording** surface for **recording** magnetically encoded **data** , wherein said **recording** surface is formatted to contain at

least one spiral **data track** , and wherein said **recording** surface is formatted to contain a plurality of angularly spaced imbedded servo patterns, said imbedded servo patterns defining a plurality of concentric **track** centerlines...

...a data transducer mounted on a movable actuator for accessing **data recorded** on said **recording** surface; and...

...a servo feedback system for **positioning** said **data** transducer to follow said spiral **data track** , wherein said servo feedback system derives separate **position** error **information** from each respective one of said angularly spaced imbedded servo patterns, each said **position** error **information** representing deviation of said **data** transducer from a concentric **track** centerline defined by said imbedded servo patterns, said deviation being measured at a respective one...

...said angularly spaced imbedded servo patterns, and wherein said servo feedback system adds a spiral **track position** error offset to each said **position** error **information** derived from each respective one of said angularly spaced imbedded servo patterns, said spiral **track position** error offset being a unique, discrete amount associated with each respective angularly spaced imbedded servo pattern, said unique, discrete amounts varying incrementally as a function of angular **position** of each said respective angularly spaced imbedded servo pattern on said disk...

...a **plurality** of **data** buffers, each of said buffers corresponding to a respective time interval associated with a multimedia presentation, each buffer having a respective output port for outputting multimedia **data stored** in said buffer...

...at least one mass **storage** device for storing a multimedia **data** presentation, wherein multimedia **data stored** on said mass **storage** device comprises a **plurality** of **sequentially stored data** segments, each **data** segment being associated with one of said time intervals...

...wherein a **plurality** of **data** segments is associated with each said time interval, and wherein successive **sequentially stored - data** segments on said at least one mass **storage** device are associated with different ones of said time intervals, the data segments associated with a particular one of said **plurality** of time intervals being **interleaved** among **data** segments associated with other time intervals ...

...at least one data bus connected to said at least one mass **storage** device for communicating multimedia **data** from said at least one mass **storage** device to said buffers...

...a **plurality** of switches connecting said **data** bus with said **plurality** of **data** buffers, each switch being associated with a respective one of said data buffers; and...

...a **controller** for operating said plurality of switches, said **controller** causing a switch associated with a selected data buffer to close when said at least one mass **storage** device outputs a **data** segment on said **data** bus associated with said a time interval corresponding to the selected data buffer...

...Title Terms: **STORAGE** ;

29/3,K/43 (Item 43 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008954634
WPI Acc No: 1992-081903/199211
XRPX Acc No: N92-061464
Optical disc recording **appts. for non contact** data **reproduction - has** memory **storing** input **digital** data **compressed from continuous signal with abnormality detectiocircuit to inhibit** recording
Patent Assignee: SONY CORP (SONY)
Inventor: ANDO R; MAEDA Y; NAGASHIMA H; HIDEKI N; RYO A; YASUAKI M; ; ANDA R
Number of Countries: 026 Number of Patents: 028
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 474377	A	19920311	EP 91307448	A	19910813	199211	B
AU 9182643	A	19920227				199218	
CA 2049768	A	19920225	CA 2049768	A	19910823	199220	
BR 9103599	A	19920512	BR 913599	A	19910822	199226	
ZA 9106158	A	19920624	ZA 916158	A	19910805	199231	
CN 1060174	A	19920408	CN 91109089	A	19910823	199247	
CS 9102545	A2	19921014	CS 912545	A	19910816	199311	
US 5224087	A	19930629	US 91747182	A	19910819	199327	
AU 646483	B	19940224	AU 9182643	A	19910820	199413	
CN 1024856	C	19940601	CN 91109089	A	19910823	199530	
EP 474377	B1	19960327	EP 91307448	A	19910813	199617	
DE 69118282	E	19960502	DE 618282	A	19910813	199623	
			EP 91307448	A	19910813		
ES 2084776	T3	19960516	EP 91307448	A	19910813	199627	
RU 2095856	C1	19971110	SU 5001384	A	19910823	199826	
SG 49892	A1	19980615	SG 968414	A	19910813	199836	
PH 28201	A	19940420	PH 42983	A	19910822	199838	
JP 2000149268	A	20000530	JP 90222824	A	19900824	200033	
			JP 200010333	A	19900824		
JP 2000215455	A	20000804	JP 90222824	A	19900824	200042	
			JP 200010332	A	19900824		
CZ 287024	B6	20000816	CS 912545	A	19910816	200048	
CA 2049768	C	20001024	CA 2049768	A	19910823	200059	
KR 221437	B1	19990915	KR 9114304	A	19910820	200107	
JP 3141242	B2	20010305	JP 90222824	A	19900824	200115	
JP 2003006871	A	20030110	JP 200010332	A	19900824	200315	N
			JP 2002132186	A	19900824		
JP 2003007002	A	20030110	JP 200010333	A	19900824	200315	N
			JP 2002132187	A	19900824		
JP 3405358	B2	20030512	JP 200010332	A	19900824	200333	N
			JP 2002132186	A	19900824		
HU 221964	A	20030528	HU 912780	A	19910823	200345	
JP 3459216	B2	20031020	JP 90222824	A	19900824	200369	
			JP 200010333	A	19900824		
JP 3459215	B2	20031020	JP 90222824	A	19900824	200369	
			JP 200010332	A	19900824		

Priority Applications (No Type Date): JP 90222824 A 19900824; JP 200010333 A 19900824; JP 200010332 A 19900824; JP 2002132186 A 19900824; JP 2002132187 A 19900824
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 474377	A		23		
Designated States (Regional): AT BE CH DE DK ES FR GB IT LI NL SE					
CA 2049768	A			G11B-007/00	

BR 9103599	A		G11B-007/00	
ZA 9106158	A	48	G11B-000/00	
CN 1060174	A		G11B-020/10	
CS 9102545	A2		G11B-020/10	
US 5224087	A	18	G11B-007/00	
AU 646483	B		G11B-020/10	Previous Publ. patent AU 9182643
CN 1024856	C		G11B-020/10	
EP 474377	B1 E	21	G11B-020/10	
Designated States (Regional): AT BE CH DE DK ES FR GB IT LI NL SE				
DE 69118282	E		G11B-020/10	Based on patent EP 474377
ES 2084776	T3		G11B-020/10	Based on patent EP 474377
RU 2095856	C1	8	G11B-007/00	
SG 49892	A1		G11B-020/10	
PH 28201	A		G11B-007/00	
JP 2000149268	A	11	G11B-007/0045	Div ex application JP 90222824
JP 2000215455	A	11	G11B-007/0045	Div ex application JP 90222824
CZ 287024	B6		G11B-020/10	Previous Publ. patent CS 9102545
CA 2049768	C E		G11B-007/00	
KR 221437	B1		G11B-020/10	
JP 3141242	B2	16	G11B-020/12	Previous Publ. patent JP 4105273
JP 2003006871	A	14	G11B-007/0045	Div ex application JP 200010332
JP 2003007002	A	13	G11B-020/12	Div ex application JP 200010333
JP 3405358	B2	14	G11B-020/10	Div ex application JP 200010332 Previous Publ. patent JP 2003006871
HU 221964	A		G11B-020/10	
JP 3459216	B2	11	G11B-007/0045	Div ex application JP 90222824 Previous Publ. patent JP 2000149268
JP 3459215	B2	11	G11B-007/0045	Div ex application JP 90222824 Previous Publ. patent JP 2000215455

Optical disc recording **appts. for non contact** data **reproduction...**

...has memory **storing** input **digital** data **compressed from continuous signal with abnormality detectiocircuit to inhibit** recording

...Abstract (Basic): The appts. **records** on an optical disc (2) having a **memory** (14) for storing **input** digital **data** compressed from a continuous signal. A signal encoder (15) arranges **data** from **memory** (14...

...The arrangement is multiple clusters at an interval of a set number of **sectors** annexing to each a linking **sector** . The cluster **data** is **interleaved** for the **recording** circuit (3, 4...

...An abnormality detection circuit (30) acts through a **controller** (7) to inhibit **recording** upon detection of abnormality. This performs a read out control of the **memory** .

...Abstract (Equivalent): An optical disc **recording** apparatus for **recording** digital **data** on a disc-shaped **recording** medium (2) by optical means, the apparatus comprising: **memory** means (14) in which **input data** digitised from continuous signals are **sequentially** written and from which the **input data** thus written are read out as **record data** having a transfer rate higher than the transfer rate of said input digital data; signal processing means (15) for arranging digital **data** read out from said **memory** means (14) into a plurality of clusters at an interval of a predetermined number of **sectors** , each cluster comprising a **plurality** of digital **data sectors** , annexing to each of said clusters a dummy **data** cluster-linking **sector** so that a linking portion to each cluster is longer than an **interleaving** length of an **interleaving** operation for said digital **data** , and for

processing the **data** of said cluster by the **interleaving** operation; **recording** means (3, 4) for **recording** digital **data** obtained from said signal processing means (15) on said medium (2); abnormality detection means (30) for detecting abnormalities in the **recording** operation in said **recording** means (3, 4); resetting control means (7) for inhibiting said **recording** operation and for resetting said **recording** means (3, 4) from an abnormal state to a normal state in dependence upon detection of an abnormality by said abnormality detection means (30); **memory** control means (7) for performing a read-out control of said **memory** means (14) for reading a predetermined amount of said **recording** **data** on a cluster-by-cluster basis when an amount of said **input** digital **data** **stored** in said **memory** means (14) exceeds a present first predetermined amount of data to maintain a writable space larger than a second predetermined amount of **data** in said **memory** means (14); and **recording** control means (7) for performing a **recording** **position** control for continuously **recording** the digital **data** intermittently read out cluster by cluster from said **memory** means (14) by said **memory** control means (7) on a **recording** **track** of said medium (2...

...Abstract (Equivalent): The optical disc **recording** appts. includes a **memory** control **device** for performing a readout control of the **memory** for reading a predetermined amount of the **recording** **data** on a cluster-by-cluster basis when an amount of the **input** digital **data** **stored** in the **memory** exceeds a present first predetermined amount of **data** , to maintain a writable space larger than a second predetermined amount of **data** in the **memory** . A **recording** unit continuously 1records digital **data** encoded by the signal processor on a **recording** **track** of the disc-shaped **recording** medium...

...An abnormality detector detects abnormalities in the **recording** operation. A resetting control device is connected to the **recording** and abnormality detector for inhibiting the **recording** operation and for resetting the **recording** unit from an abnormal state to a normal state upon detection of an abnormality by...

...USE - For recording compressed digital **information** to optical disc...

...Title Terms: **RECORD** ;

29/3,K/44 (Item 44 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008939271 **Image available**
WPI Acc No: 1992-066540/199209
XRPX Acc No: N92-049966
Disc recording **and reproducing appts. for time compressed digital** data **- uses temporary** store **to read out multiple clusters that are annexed at linking portions with** sector **longer than** interleaving data **length**
Patent Assignee: SONY CORP (SONY)
Inventor: ANDO R; FUJIIE K; FUJISAWA H; MAEDA Y; MUKAWA H; NAGASHIMA H; OBATA H; YOSHIDA T
Number of Countries: 016 Number of Patents: 015
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 472343	A	19920226	EP 91307446	A	19910813	199209 B
AU 9182650	A	19920227				199218
CA 2049280	A	19920225	CA 2049280	A	19910815	199220
CN 1059224	A	19920304	CN 91105980	A	19910823	199243
US 5243588	A	19930907	US 91746787	A	19910816	199337
AU 646879	B	19940310	AU 9182650	A	19910820	199415
US 5363362	A	19941108	US 91746787	A	19910816	199444
			US 9348359	A	19930415	
CN 1026532	C	19941109	CN 91105980	A	19910823	199544
EP 472343	B1	19960320	EP 91307446	A	19910813	199616
DE 69118050	E	19960425	DE 618050	A	19910813	199622
			EP 91307446	A	19910813	
RU 2054203	C1	19960210	SU 5001474	A	19910823	199645
SG 49885	A1	19980615	SG 968142	A	19910813	199836
CA 2049280	C	20001031	CA 2049280	A	19910815	200060
JP 3141241	B2	20010305	JP 90222821	A	19900824	200115
KR 242901	B1	20000201	KR 9114301	A	19910820	200118

Priority Applications (No Type Date): JP 90222821 A 19900824
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 472343	A				
Designated States (Regional): AT CH DE FR GB IT LI NL					
CA 2049280	A			G11B-007/00	
CN 1059224	A			G11B-020/12	
US 5243588	A		15	G11B-005/09	
AU 646879	B			G11B-007/00	Previous Publ. patent AU 9182650
US 5363362	A		15	G11B-005/09	Div ex application US 91746787 Div ex patent US 5243588
CN 1026532	C			G11B-020/12	
EP 472343	B1	E	19	G11B-007/00	
Designated States (Regional): AT CH DE FR GB IT LI NL					
DE 69118050	E			G11B-007/00	Based on patent EP 472343
RU 2054203	C1		7	G11B-027/00	
SG 49885	A1			G11B-007/00	
CA 2049280	C	E		G11B-007/00	
JP 3141241	B2		14	G11B-020/12	Previous Publ. patent JP 4105271
KR 242901	B1			G11B-007/00	

Disc recording **and reproducing appts. for time compressed digital** data **- ...**

...uses temporary store **to read out multiple clusters that are annexed at**

linking portions with sector **longer than** interleaving data **length**

...Abstract (Basic): The equipment includes a **store** (14) for temporarily storing digital **data** . Digital **data** is arranged (15) to read out from the **store** into multiple of clusters. They are arranged at an interval of set **sectors** . Cluster linking **sections** are annexed at linking portions of each of the clusters. Each cluster-linking **sector** is longer than an **interleaving** length for the digital **data** .

...

...The digital data is processed within each of the clusters by **interleaving** and **recording** **interleaved** **data** on the medium (2...

...USE - For optically **recorded** digital **data** . (19pp Dwg.No.1/9)

...Abstract (Equivalent): A disc **recording** apparatus for **recording** time compressed digital **data** on a disc-shaped **recording** medium (2), the apparatus comprising: **storage** means (14) for temporarily storing **input** **data** digitized from continuous signals **sequentially** written thereto and from which the **input** **data** thus written are read out as **record** **data** having a transfer rate higher than the transfer rate of said input digital data; and means (15) for arranging said digital **data** read out from said **storage** means (14) into a plurality of clusters (C) means (15) for arranging said digital **data** read out from said **storage** means (140 into a plurality of clusters (C) at an interval of a predetermined number of **sectors** , each cluster comprising a **plurality** of digital **data** **sectors** , annexing dummy **data** cluster-linking **sectors** at linking portions of each of said clusters (C), each of said cluster-linking **sectors** being longer than an **interleaving** length for said digital **data** subsequently processing the **data** within each of said clusters (C) by **interleaving** , and **recording** **interleaved** **data** on said medium (2...

...Abstract (Equivalent): compressed digital data are arranged in clusters at an interval of a predetermined number of **sectors** . A cluster-linking **sector** having a length longer than an **interleaving** length is provided at each linking part of each cluster, and the digital **data** are subsequently **interleaved** and **recorded** on a disc-shaped **recording** medium so that **interleaving** at the time of **data** **recording** on the cluster-by-cluster basis is within the range of the cluster-linking **sector** .

...

...Appts. is provided for reproducing digital data by an optical unit in which playback **data** are obtained by reproducing **record** **data** **recorded** on a disc-shaped **recording** medium in such a manner that a cluster-linking **sector** longer than an **interleaving** length is provided in a linking **section** of each cluster composed of a predetermined number of **sectors** .

...

...ADVANTAGE - Continuous **recording** and reproduction for sufficiently long time is possible even with use of small disc. Processing complexity due to **interleaving** at time of **recording** compressed audio **data** on disc avoided...

...The apparatus for processing digital **data** to be **recorded** on a disc-shaped **recording** medium includes a **storage** device for transiently storing the digital **data** and a device for **sequentially** reading out bursts of the digital **data** from the **storage** device. Each of the bursts includes a cluster of a predetermined number of **sectors** of **data** , and cluster linking **sectors** concatenated with the cluster. An **interleaving** device receives and processes each of the

bursts, by **interleaving** cluster **data** in accordance with an **interleaving** period, for **recording** on the disc-shaped **recording** medium. The cluster linking **sectors** concatenated with the cluster of each of the bursts have time duration longer than the **interleaving** period...

...A **controller** is provided for controlling readout of the **storage** device. The **controller** operates in a mode in which, when the **storage** device contains more than a first predetermined amount of data, the **controller** causes a first amount of digital **data** to be continuously read from the **storage** device to perpetual maintain a **writing** space in excess of a second predetermined amount of **data** in the **storage** device...

...USE/ADVANTAGE - for optical disc e.g. CD. Allows continuous **recording** and reproduction for sufficient time even with small disc e.g. over 70 min. Avoids processing complexity due to **interleaving** at **recording** compressed audio **data** . Minimises changes in control or signal processing operations brought about as result of switching selection

...Title Terms: **RECORD** ;

29/3,K/48 (Item 48 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007714333 **Image available**
WPI Acc No: 1988-348265/198849
Related WPI Acc No: 1991-255137; 1991-269410; 1991-269411; 1991-269412
XRPX Acc No: N88-263948
Data processing e.g. for personal computer or word processor - holding commands from host computer in controller register **and handling double-encoded** interleaved data **by error correction processor**
Patent Assignee: SONY CORP (SONY)
Inventor: FURUHASHI M; YAMAOKA K
Number of Countries: 009 Number of Patents: 020
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2205423	A	19881207	GB 8812941	A	19880601	198849	B
DE 3818881	A	19890112	DE 3818881	A	19880603	198904	
JP 63302628	A	19881209	JP 87139122	A	19870603	198904	
AU 8816760	A	19881208				198905	
FR 2616247	A	19881209				198905	
GB 2205423	B	19920219				199208	
AU 9210813	A	19920416	AU 9210813	A	19920207	199225	
			AU 8816760	A	19880000		
AU 9210814	A	19920416	AU 9210814	A	19920207	199225	
			AU 8816760	A	19880000		
AU 9210815	A	19920416	AU 9210815	A	19920207	199225	
			AU 8816760	A	19880000		
CA 1317029	C	19930427	CA 568383	A	19880602	199322	
CA 1321651	C	19930824	CA 568383	A	19880602	199340	
			CA 616299	A	19920124		
CA 1321837	C	19930831	CA 568383	A	19880602	199341	
			CA 616298	A	19920124		
CA 1325282	C	19931214	CA 568383	A	19880602	199405	
			CA 616297	A	19920124		
US 5287468	A	19940215	US 88201414	A	19880602	199407	
			US 91784144	A	19911030		
AU 648639	B	19940428	AU 9210814	A	19920207	199422	
			AU 8816760	A	19880000		
AU 648640	B	19940428	AU 9210815	A	19920207	199422	
			AU 8816760	A	19880000		
AU 648866	B	19940505	AU 9210813	A	19920207	199423	
			AU 8816760	A	19880000		
SG 9500265	A	19951222	SG 95265	A	19950217	199611	
US 5548599	A	19960820	US 88201414	A	19880602	199639	
			US 90580332	A	19900910		
			US 93103824	A	19930809		
KR 120823	B1	19971029	KR 886685	A	19880603	199948	

Priority Applications (No Type Date): JP 87201031 A 19870813; JP 87139122 A 19870603; JP 87139124 A 19870603
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2205423	A		83		
AU 9210813	A			G06F-011/08	Div ex application AU 8816760
AU 9210814	A			G06F-009/22	Div ex application AU 8816760
AU 9210815	A			G06F-011/08	Div ex application AU 8816760
CA 1321651	C			G06F-013/12	Div ex application CA 568383
CA 1321837	C			G06F-013/12	Div ex application CA 568383
CA 1325282	C			G06F-011/08	Div ex application CA 568383
US 5287468	A		27	G06F-009/22	Cont of application US 88201414

AU 648639	B		G06F-009/22	Div ex application AU 8816760 Previous Publ. patent AU 9210814
AU 648640	B		G06F-011/08	Div ex application AU 8816760 Previous Publ. patent AU 9210815
AU 648866	B		G06F-011/08	Div ex application AU 8816760 Previous Publ. patent AU 9210813
SG 9500265	A			Previous Publ. patent GB 2241363
US 5548599	A	26	G11B-020/18	Div ex application US 88201414 Cont of application US 90580332
CA 1317029	C		G06F-003/06	
KR 120823	B1		G06F-011/00	

... **holding commands from host computer in** controller register **and handling double-encoded** interleaved data **by error correction processor**

...Abstract (Basic): The data processing method involves storing simplified commands from a host computer in a command **register** , interpreting the commands into a series of microprograms and receiving or transmitting the information data from or to the host computer. The **information data** processed for **storage** or retrieval into or from a **recording** medium according to the series of microprograms...

...The apparatus includes **register** for storing simplified commands from a host computer and a device for interpreting the commands...

...provided for receiving or transmitting the information data from or to the host computer. The **data** is processed for **storage** or retrieval into or from a **recording** medium according to the series of microprograms...

...ADVANTAGE - Error correction capability for burst errors is improved. **Data** can be **recorded** or reproduced efficiently without lowering processing efficiency of host computer...

...Abstract (Equivalent): codes being transmitted a plurality of times, the method comprising the steps of; receiving the **information data** a **plurality** of times; and decoding the error detection or correction codes of the received information data...

...Abstract (Equivalent): An apparatus for reproducing error correction encoded **information** data recorded on tracks of a **recording** medium under the control of a host computer, comprising...

...means for receiving from the host computer, at a first time, a first **track** number of a first **track** from which first **recorded** error correction encoded **information data** is to be reproduced, and, at a second time, a second **track** number of a second **track** from which second **recorded** error correction encoded **information data** is to be reproduced...

...means for moving a reproducing pickup means with regard to the **recording** medium to the first **track** or to the second **track** ;
...

...means for reproducing the first **recorded** error correction encoded **information data** from the **recording** medium as a reproduced signal
...

...a **memory** for storing the first error correction encoded **information** data; and...

...means for decoding error correction codes of the **stored** first error correction encoded **information data** during movement of the

reproducing pickup means to the second **track** .

...

...The **data** processing system has an external **data storage** medium, and includes a host computer generating macrocommand instructions for initiating **data** transfer between the host computer and the **storage** medium. Each macrocommand instruction represents series of predetermined instructions to be executed as a microprogram routine. A **memory stores data** from the host computer for subsequent **recording** on the **storage** medium and **stores data** reproduced from the **storage** medium for subsequent supply to the host computer...

...A **memory controller** responds to a respective set of microprogram instruction steps to control the supply of the **data** to and from the **memory** and includes control **data storage** to indicate a start **address** in the **memory** and a desired number of **data** to be transferred. The **data** transferred to and from the **memory** is **stored** in and retrieved from, respectively, **addresses** in the **memory** starting from the start **address** and having a number corresponding to the number of data to be transferred...

...ADVANTAGE - Lower control dependency on host computer; **recording** /reproduction performed efficiently without lowering processing efficiency of host computer; error correction capability for burst

...Title Terms: **REGISTER** ;

29/3,K/51 (Item 51 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004332432
WPI Acc No: 1985-159310/198526
XRPX Acc No: N85-120121
Disc reproducing apparatus with RAM controller **- has** memory **for storing main and subsidiary digitally reproduced** data
Patent Assignee: SONY CORP (SONY); FURUYA T (FURU-I)
Inventor: FURUKAWA S; FURUYA T; HORI K
Number of Countries: 016 Number of Patents: 012
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8502707	A	19850620	WO 84JP594	A	19841214	198526	B
AU 8537811	A	19850626				198536	
BR 8407223	A	19851126				198602	
EP 166785	A	19860108	EP 85900188	A	19850000	198602	
HU 37520	T	19851227				198607	
DK 8503715	A	19850815				198630	
US 4977550	A	19901211	US 88291415	A	19881222	199101	
EP 166785	B	19920304				199210	
DE 3485541	G	19920409				199216	
KR 9210188	B1	19921119	WO 84JP594	A	19841214	199414	
			KR 85700166	A	19850816		
DK 169452	B	19941031	WO 84JP594	A	19841214	199442	
			DK 853715	A	19850815		
SG 9590375	A	19950818	SG 9590375	A	19950301	199544	

Priority Applications (No Type Date): JP 83243486 A 19831223; JP 83237370 A 19831216
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8502707	A	J	29		
Designated States (National): AU BE DK HU KR US					
Designated States (Regional): AT CH DE FR GB NL SE					
EP 166785	A	E			
Designated States (Regional): AT CH DE FR GB LI NL SE					
EP 166785	B				
Designated States (Regional): AT CH DE FR GB LI NL SE					
DK 169452	B			G11B-020/10	Previous Publ. patent DK 8503715
SG 9590375	A				Previous Publ. patent EP 166785
KR 9210188	B1			G11B-020/10	

Disc reproducing apparatus with RAM controller **- ...**

...**has** memory **for storing main and subsidiary digitally reproduced** data

...Abstract (Basic): The apparatus generates a **write** clock synchronised with a disk reproducing signal, and a read clock having a predetermined period. A buffer **memory** has the main and subsidiary digital **data** , which have been reproduced from the disk, written and read out in response to the read clock, and effects de- **interleaving** of the main digital **data** .
...

...A control device is adapted for finding the reproduction **position** of the main digital **data** in accordance with the subsidiary digital **data** read out from the buffer **memory** . Further, a buffer **memory** into which the subsidiary **data** is written may be constituted by an FIFO

buffer **register** which is provided separately from the buffer **memory** .

...Abstract (Equivalent): on which main digital data and subsidiary digital data for selectively reproducing the main digital **data** are **recorded** in **multiplex** fashion, the apparatus comprising a disc playback device for reproducing said main digital data and...

...and for receiving said reproduced main digital data and subsidiary digital data and subsidiary digital **data** ; a decoding circuit including a **write** clock generating circuit (23,24) conencted to said **input** circuit for generating a **write** clock synchronised with said reproduced main digital **data** , a read clock generating circuit (31,32) for generating a read clock having a predetermined period, and a **memory** ciruit (25) connected to said **input** circuit (21) for having said reproduced main digital data written therein and read therefrom in response, respectively, to **write address data** and read **address data** corresponding to said **write** clock and said read clock so that reproduced main digital **data** is de- **interleaved** to be decoded; and a control circuit (35) connected to said disc playback device and for searching a **position** to be reproduced of said reproduced main digital data on the basis of said reproduced subsidiary digital **data** ; wherein said **memory** circuit (25) also has said reproduced subsidiary digital data written therein without said reproduced subsidiary date having been separated from said main digital **data** in response to said **write address data** and read **address data** corresponding to said **write** clock and said read clock, respectively, and a decoding circuit (30) is provided connected to said **memory** circuit (25) for receiving said reproduced subsidiary digital **data** from said **memory** circuit (25) and for separating said reproduced subsidiary digital data from said reproduced main digital...

...Abstract (Equivalent): The apparatus playbacks from a disc main digital data and subsidiary digital **data** to reproduce the main digital **data recorded** in **multiplex** fashion. The appts. incorporates a **write** clock generator for generating a clock synchronized with a reproduced signal from the disc. A read clock generator generates a read clock with a predetermined period. A buffer **memory** is provided into which main digital **data** and subsidiary signal data reproduced from the disc are written and read out in response to the read clock so as to de-**interleave** the main digital **data** .

...

...A control unit seeks a **position** to be reproduced in the main digital **data** in response to the subsidiary digital **data** read out from the buffer **memory** . The buffer **memory** into which the subsidiary digital **data** is written is a FIFO buffer **register** which is provided separately from the buffer **memory** into which the main digital date is written

...Title Terms: **MEMORY** ;

29/3,K/53 (Item 53 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004051473
WPI Acc No: 1984-197015/198432
XRPX Acc No: N84-147115
Video switching system for asynchronous digital transmission - uses common bus for terminals for transmission of data packet **of** identifiers **for** addressing **purposes**
Patent Assignee: DEVAULT M (DEVA-I); GERALD B (GERA-I)
Inventor: GERARD B; ROUAUD Y
Number of Countries: 012 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2538984	A	19840706	FR 8222122	A	19821230	198432	B
JP 59135954	A	19840804	JP 8413	A	19840104	198437	
EP 126196	A	19841128	EP 83402566	A	19831230	198448	
US 4566095	A	19860121	US 83566433	A	19831228	198606	
CA 1211824	A	19860923				198643	
EP 126196	B	19870616				198724	
DE 3372156	G	19870723				198730	

Priority Applications (No Type Date): FR 8222122 A 19821230
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2538984	A		25		
EP 126196	A	F			
Designated States (Regional): BE CH DE GB IT LI NL SE					
EP 126196	B	F			
Designated States (Regional): BE CH DE GB IT LI NL SE					

... **uses common bus for terminals for transmission of** data packet **of** identifiers **for** addressing **purposes**

...Abstract (Basic): He) and frame sync (Se) signals are also obtained. The frame sync. signal resets a **sequence** generator (112). The **data** is then **recorded** in 8 bit words in **registers** (135,136) and into two other **registers** (133,134) through a multiplexer (132...

...A wait file (14) using a RAM (141) is controlled from a **controller** (142) which generates the **addresses** and read or **write** signals. This ensures that **data** flow constraints are **accounted** for. Input (143) and output (144,145) **registers** provide temporary **storage** for synchronisation of the access **memories** . A bus access unit (15) contains a **sequencer** (151) which ensures that a complete **data packet** is ready for transmission on the bus...

...USE - For point to point communication of **integrated information** channels. (25pp twg.No.0/13...

...Time division multiplex switching network for asynchronous digital transmission system comprising: a plurality of incoming **multiplex** highways each including asynchronous channels carrying **packets** made up of **data** and a label and a **plurality** of outgoing **multiplex** highways each including asynchronous channels carrying **packets** made up of data and a label incoming and outgoing switching terminal equipments respectively connected...

...is in the respective in incoming switching terminal equipment converted by means of a control **memory** into an **identifier** intended to be

decode din the outgoing switching terminal equipment and composed of three words...

...to be switched to several calling parties, a second word selecting the number of the **addressed** outgoing multiplex highway or not having any significance according to the first word value, and a third word characterising the number of the **address** outgoing asynchronous channel of the numbers of several outgoing asynchronous channels in the case of a diffusing switching and in that means for decoding the **identifier** are provided in each outgoing switching terminal equipment in order to allow, on the one...

...intended for said equipment as a function of the second and third words of the **identifier** and, on the other hand, to a control memroy in said equipment, to process the...

...Abstract (Equivalent): Time division multiplex switching network for asynchronous digital transmission system comprising: a plurality of incoming **multiplex** highways each including asynchronous channels carrying **packets** made up of **data** and a label and a **plurality** of outgoing **multiplex** highways each including asynchronous channels carrying **packets** made up of data and a label incoming and outgoing switching terminal equipments respectively connected...

...is in the respective in incoming switching terminal equipment converted by means of a control **memory** into an **identifier** intended to be decode din the outgoing switching terminal equipment and composed of three words...

...to be switched to several calling parties, a second word selecting the number of the **addressed** outgoing multiplex highway or not having any significance according to the first word value, and a third word characterising the number of the **address** outgoing asynchronous channel of the numbers of several outgoing asynchronous channels in the case of a diffusing switching and in that means for decoding the **identifier** are provided in each outgoing switching terminal equipment in order to allow, on the one...

...intended for said equipment as a function of the second and third words of the **identifier** and, on the other hand, to a control memroy in said equipment, to process the...

...Abstract (Equivalent): switching, data switching between a single calling party and a number of called parties, and **data** switching between **several** calling parties and a single called party. The network comprises several incoming and outgoing time division multiplex highways including asynchronous channels each formed by a **packet** **data** and an **address** label (j.k...

...ADVANTAGE - Economical in **memory** .

(

...Title Terms: **IDENTIFY** ;

29/3,K/55 (Item 55 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003350062
WPI Acc No: 1982-K8083E/198233
Cyclically operating data processing system - has multi-phase subroutine control providing concurrent execution of tasks
Patent Assignee: BURROUGHS CORP (BURS)
Inventor: DONSUNG R K
Number of Countries: 007 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 57313	A	19820811	EP 81304888	A	19811020	198233	B
US 4467410	A	19840821	US 81231554	A	19810204	198436	
EP 57313	B	19850717				198529	
DE 3171418	G	19850822				198535	
US 4649472	A	19870310	US 84589298	A	19840314	198712	

Priority Applications (No Type Date): US 81231554 A 19810204
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 57313	A	E	32		

Designated States (Regional): BE DE FR GB IT NL

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 57313	B	E			

Designated States (Regional): BE DE FR GB IT NL

...Abstract (Basic): a number of tasks each including one or more subroutines. The system includes a subroutine **controller** having a return **address store** for each tank and a return **address** control responsive to a subroutine entry indication and a task **identification** indication when a task arrives at the beginning of a subroutine- for determining a return **address** for the indicated subroutine and for storing this return **address** in the corresponding **store** . The control is also responsive to the same indications when a task arrives at the end of a subroutine for causing a particular return **address stored** in the respective **store** to be accessed and applied to the system...

...a number of successive cycles so as to permit the storing and accessing of return **addresses** w.r.t. the **store** to occur concurrently in a phased manner for a number of tasks.
...Abstract (Equivalent): A subroutine control circuit for the receipt, **storage** and ordered retrieval of a **sequence** of subroutine return **addresses** (RA) for a corresponding linked and nested **sequence** of subroutines in a **data** processing system including a **plurality** of **data** processors controlled by a common clock signal, each of said processors being operable to perform one out of a corresponding **plurality** of simultaneously **interleaved data** processing operations each consisting in the performance on successive cycles of said common clock signal...

...of processors where each of said plurality of processors is coupled to provide said return **address** (RA) to said circuit in the form of a present microinstruction **address** (PA) together with an **address** offset to be added to said present micro-instruction **address** to provide said return **address**
...

...s (RA), each of said processors utilizing a micro-programme **sequence** of independently **addressable** microinstructions, said circuit

including a stack **store** (50) coupled to receive an **input** return **address** (RA3) from said system, operable to **store** said **input** return **address** (RA3) in response to the receipt from said system of subroutine entry indication (E3), and...

...said system of a subroutine return indication (R3) to prpvide as output the next previously **stored** retrieved return **address** (RA), said circuit being characterized by comprising a plurality of stages (S-1,S-2

...Abstract (Equivalent): subroutine hardware includes a multi-level stack for each task and a fast access return **address register** which permits a return **address** to be rapidly made available when required during execution of a task...

...subroutine hardware includes a multi-level stack for each task and a fast access return **address register** which permits a return **address** to be rapidly made available when required during execution of a task ...

29/3,K/64 (Item 64 from file: 347)
DIALOG(R)File 347:JAPIO

03041345 **Image available**
DATA COMMUNICATION EQUIPMENT FOR VEHICLE

PUB. NO.: 02-016845 [JP 2016845 A]
PUBLISHED: January 19, 1990 (19900119)
INVENTOR(s): ABE NORIYUKI
APPLICANT(s): NISSAN MOTOR CO LTD [000399] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-165993 [JP 88165993]
FILED: July 05, 1988 (19880705)
JOURNAL: Section: E, Section No. 909, Vol. 14, No. 161, Pg. 22, March 28, 1990 (19900328)

ABSTRACT

... reduce the burden of a control processing and to simplify equipment constitution by executing the **writing** and reading of **data** with common **memories integrated** in **plural** communication equipments...

...CONSTITUTION: CPU outputs **data** to be written to a **write data register** 57 through a **data** bus 21a, outputs **address information** to an indirect **register** 53 and outputs a **write** signal WR through a **write** line 17a. When the signal WR is **inputted** through the line 17a, an access timing **controller** 43 outputs a **memory write** signal 43e to a decentralized shared **memory** 45, and an **address** decoder 55 outputs **address information** from the **register** 53 to the **memory** 45. A **controller** 43 outputs an output switching signal 43c to the decoder 55 and outputs **address information** from the decoder 55 only in the period when the signal 43c is in H. The **controller** 43 outputs the signal to the **register** 57 in synchronism with the period of H of the signal 43c. The **register** 57 outputs **data information** from CPU11a to the **memory** 45 in synchronism with an output enable signal 43a and **stores data information** from the **register** 57 with respect to the **address** which the **register** 53 has designated.

29/3,K/65 (Item 65 from file: 347)
DIALOG(R)File 347:JAPIO

02335003 **Image available**
DATA RECORDING SYSTEM FOR NUMERICAL **CONTROLLER**

PUB. NO.: 62-251903 [JP 62251903 A]
PUBLISHED: November 02, 1987 (19871102)
INVENTOR(s): SAKAMOTO EIICHIRO
TANIGUCHI RYOSAKU
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-096330 [JP 8696330]
FILED: April 25, 1986 (19860425)
JOURNAL: Section: P, Section No. 692, Vol. 12, No. 129, Pg. 78, April 21, 1988 (19880421)

DATA RECORDING SYSTEM FOR NUMERICAL **CONTROLLER**

ABSTRACT

PURPOSE: To **integrate plural** various kinds of information in a single **file** by identifying production **information records** and control **data records** with respective **record** numbers of **records** constituting the **file** formed on a **storage** medium...

...CONSTITUTION: Numerical control **data** is **stored** in even **records** constituting a **file** having **file** number 1 of numerical control **data**, and production **information** is **stored** in odd **records**. A **record** is read out from a **magnetic disk** 1a by the request from a numerical control NC device **controller** 2, and it is discriminated whether the current **record** number is odd or not. If not, **data** in this **record** is discriminated as numerical control **data** to save the **memory** of a personal computer PC 1. If it is odd, the **record** is skipped. When all **records** are read out, the **file** is closed, and control data is transferred from the PC 1 to the **controller** 2 and is transferred furthermore to an NC device 3.

34/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016403020 **Image available**
WPI Acc No: 2004-560931/200454
XRPX Acc No: N04-443850
Prefetch generating method for e.g. computer system, involves speculatively executing code through thread and issuing prefetch for memory **reference to load cache line into cache if target reference** address **is resolved**
Patent Assignee: SUN MICROSYSTEMS INC (SUNM); CHAUDHRY S (CHAU-I); TREMBLAY M (TREM-I)
Inventor: CHAUDHRY S; TREMBLAY M
Number of Countries: 107 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040133767	A1	20040708	US 2002436492	P	20021224	200454	B
			US 2003741949	A	20031219		
WO 200459473	A2	20040715	WO 2003US40598	A	20031219	200454	
AU 2003303438	A1	20040722	AU 2003303438	A	20031219	200476	

Priority Applications (No Type Date): US 2002436492 P 20021224; US 2003741949 A 20031219
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040133767	A1		10	G06F-009/00	Provisional application US 2002436492
WO 200459473	A2	E		G06F-009/40	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BW BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NI NO NZ OM PG PH PL PT RO RU SC SD SE SG SK SL SY TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
Designated States (Regional): AT BE BG BW CH CY CZ DE DK EA EE ES FI FR GB GH GM GR HU IE IT KE LS LU MC MW MZ NL OA PT RO SD SE SI SK SL SZ TR TZ UG ZM ZW

AU 2003303438	A1		G06F-009/40	Based on patent WO 200459473

... **for e.g. computer system, involves speculatively executing code through thread and issuing prefetch for** memory **reference to load cache line into cache if target reference** address **is resolved**

Abstract (Basic):
... The method involves executing code via one **thread** running on a processor supporting simultaneous **multithreading** . The code from the point of a stall is speculatively executed through another thread upon encountering the stall during code execution via former thread. A prefetch is issued for a **memory** reference to load a cache line into a cache if the target **address** for the reference is resolved upon encountering the reference.
... Used for generating a prefetch **stored** in a computer readable **storage** medium e.g. **disk** drive, **magnetic tape** , CD, and DVD, of a computer system, a mainframe computer, a digital signal processor, a portable computing device, a personal organizer, a device **controller** , and a computational engine...

...other long latency instructions during the speculative execution, because the instructions are unlikely to affect **address** computations. The prefetch operations performed during the speculative execution are

likely to improve subsequent system performance during non-speculative execution. Instructions update a shadow **register** file instead of updating an architectural **register** file during speculative execution of the code so that the execution does not affect the architectural sate of the processor. The processor supports simultaneous **multithreading** , which enables **multiple threads** to execute concurrently through time- **multiplexed interleaving** in a single processor pipeline...

...Title Terms: **MEMORY** ;

34/3,K/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016319217 **Image available**
WPI Acc No: 2004-477112/200445
XRPX Acc No: N04-375848
Memory packets interleaving **method for network processing device e.g. router, involves accessing** memory **banks in** sequence **based on clock cycle** sequencing **to precharge banks while other banks are being accessed during** memory **cycle**
Patent Assignee: FORCE 10 NETWORKS INC (FORC-N)
Inventor: LEE E; SIKDAR S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6745277	B1	20040601	US 2000679266	A	20001004	200445	B

Priority Applications (No Type Date): US 2000679266 A 20001004
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6745277	B1		12	G06F-012/00	

Memory packets interleaving **method for network processing device e.g. router, involves accessing** memory **banks in** sequence **based on clock cycle** sequencing **to precharge banks while other banks are being accessed during** memory **cycle**

Abstract (Basic):
... The method involves **identifying** any of multiple **writes** and multiple reads for a **memory** cycle that needs to access the same **memory** banks. Clock cycles are **sequenced** for the **identified writes** and reads during the **memory** cycle. The banks are accessed during the **memory** cycle in **sequence** based on the **sequencing** so that the banks are precharged during the cycle while other banks are being accessed...
... Used for **interleaving packets** in a **memory** having **multiple memory** banks (claimed) of a network processing device e.g. router, switch, concentrator, and gateway...

...The **interleaving** method is intelligent and preserves the **memory** bus bandwidth that would normally be wasted accessing the **memory** banks...
...The drawing shows a system **controller** in a network processing device ...

... **Memory** (114...

... 1Interleave scheduler (116
Title Terms: **MEMORY** ;

34/3,K/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

013445907 **Image available**
WPI Acc No: 2000-617850/200059
XRPX Acc No: N00-457768
Simultaneous data **transferring method for** data **processing, involves transferring** stored , **coalesced** packet data **from** data **buffer to** data **path in response to** write **enable signal**
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: LAVELLE M G; LYNCH W L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6078587	A	20000620	US 97880469	A	19970623	200059	B

Priority Applications (No Type Date): US 97880469 A 19970623
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6078587	A		12	H04L-012/28	

Simultaneous data **transferring method for** data **processing, involves transferring** stored , **coalesced** packet data **from** data **buffer to** data **path in response to** write **enable signal**

Abstract (Basic):
... Mask **information stored** in a mask information buffer and mask **information** from a next packet in **several data packets** is utilized to assert a **write** enable signal. In response to assertion of **write** enable signal, the **packet data** from the next **data packet** is **stored** and then the **stored coalesced packet data** is transferred to the **data** path.
... The **write** enable signal indicates that **packet data** from the next **data packet** would not overwrite valid **packet data stored** in **data** buffer and also indicate whether the **data** from the next **packet** is within the **locus** of permissible **locations** . An INDEPENDENT CLAIM is also included for a **data coalescing** system...

...Since **data** is collected from **multiple data packet** for group transfer on **data** path, the data transfer bandwidth on data path way is utilized to a maximum extent...

...The figure shows the schematic block diagram showing overall data flow in graphics **controller** .

...Title Terms: **STORAGE** ;

34/3,K/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012325508 **Image available**
WPI Acc No: 1999-131615/199911
Related WPI Acc No: 1996-414640
XRPX Acc No: N99-095912

Data **blocks exchanging method between** memory **and I/O devices in** data **processing system - involves** interleaving **blocks of** data **by transferring** data **corresponding to one** memory **table and then transferring** data **corresponding to another** memory **table**

Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: CARMICHAEL R D; WARD J M; WINCHELL M A

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5864712	A	19990126	US 95407439	A	19950317	199911 B
			US 95488427	A	19950607	
			US 96777858	A	19961231	

Priority Applications (No Type Date): US 95488427 A 19950607; US 95407439 A 19950317; US 96777858 A 19961231
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5864712	A		30	G06F-013/10	CIP of application US 95407439 Cont of application US 95488427

Data **blocks exchanging method between** memory **and I/O devices in** data **processing system**...

...**involves** interleaving **blocks of** data **by transferring** data **corresponding to one** memory **table and then transferring** data **corresponding to another** memory **table**

...Abstract (Basic): NOVELTY - Two I/O devices are associated with respective **memory** tables (137,139). The blocks of **data** are **interleaved** by transferring **data** corresponding to first **memory** table and then transferring **data** corresponding to second **memory** table. One of the I/O devices is selected, and a portion of **data** is exchanged between the selected I/O **device** and **memory sequentially** until all the **data** is exchanged. DETAILED DESCRIPTION - An INDEPENDENT CLAIM for I/O control device is also included...

...ADVANTAGE - Provides I/O control device with **data** management component capable of processing **multiple** PRD tables. DESCRIPTION OF DRAWING(S) - The figure shows mechanism for performing single data **manager** controlled bus master gathering DMA operations in two I/O channel system. (137,139) **Memory** tables...

...Title Terms: **MEMORY** ;

34/3,K/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011034431 **Image available**
WPI Acc No: 1997-012355/199701
XRPX Acc No: N97-010690
Reconfigurable deinterleaving appts. for data streams - is selectively configurable for data **streams** interleaved **according to one of** several interleaving **schemes using several parameter sets with each set corresponding to particular deinterleaving algorithm**
Patent Assignee: ADVANCED HARDWARE ARCHITECTURES INC (ADHA-N)
Inventor: BERGE T; ZWEIGLE G
Number of Countries: 019 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9637050	A1	19961121	WO 96US4758	A	19960404	199701	B

Priority Applications (No Type Date): US 95441078 A 19950515
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9637050	A1	E	20	H03M-013/22	

Designated States (National): CA JP
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

... **is selectively configurable for** data **streams** interleaved **according to one of** several interleaving **schemes using several parameter sets with each set corresponding to particular deinterleaving algorithm**

...Abstract (Basic): The appts. includes a data input for receiving a stream of **data** that was **interleaved** according to one of **several interleaving** algorithms. A control **input** receives a signal for selectively configuring the appts. to deinterleave the stream of **interleaved data** according to a predetermined deinterleaving algorithm. An **interleaving** circuit coupled to the **data input** selectively configures the appts. to **interleave** a stream of **data** .
...

...An **interleaving** /deinterleaving appts. includes an **input** for receiving a stream of **data** bytes. A RAM has several data byte storage **locations** coupled to receive the **input** stream. A **write address** generator coupled to the **memory** directs each byte in the **input** stream to an appropriate **storage location** . A read **address** generator coupled to the **memory** selects which of the **locations** will provide a **data** byte to an output stream. An output coupled to the **memory** receives the output stream. A **controller** coupled to the **memory** , the **write address** generator and the read **address** generator includes several parameter sets. Each parameter set allows the **controller** to **interleave** or deinterleave an **input** stream according to one of **several interleaving** algorithms...

...ADVANTAGE - Appts. can be reconfigured to deinterleave streams **interleaved** according to several **interleaving** schemes. Cost effective
...Title Terms: **INTERLEAVED** ;

34/3,K/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

010917689 **Image available**
WPI Acc No: 1996-414640/199642
Related WPI Acc No: 1999-131615
XRPX Acc No: N96-349015
Block transfer method for data **from** several input **-output devices - involves scheduling DMA block transfers based upon availability of** data **from buffer** memory **of** input **and output devices**
Patent Assignee: LSI LOGIC CORP (LSIL-N); SYMBIOS LOGIC INC (SYMB-N)
Inventor: CARMICHAEL R; WARD J M; WINCHELL M A; CARMICHAEL R D
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 732659	A1	19960918	EP 96301799	A	19960315	199642	B
JP 8297628	A	19961112	JP 9660667	A	19960318	199704	
US 5894560	A	19990413	US 95407439	A	19950317	199922	
			US 96702998	A	19960826		
EP 732659	B1	20010808	EP 96301799	A	19960315	200146	
DE 69614291	E	20010913	DE 614291	A	19960315	200161	
			EP 96301799	A	19960315		

Priority Applications (No Type Date): US 95407439 A 19950317; US 96702998 A 19960826
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 732659	A1	E	22	G06F-013/28	
Designated States (Regional): DE FR GB					
JP 8297628	A		22	G06F-013/28	
US 5894560	A			G06F-013/00	Cont of application US 95407439
EP 732659	B1	E		G06F-013/28	
Designated States (Regional): DE FR GB					
DE 69614291	E			G06F-013/28	Based on patent EP 732659

Block transfer method for data **from** several input **-output devices**...

...**involves scheduling DMA block transfers based upon availability of** data **from buffer** memory **of** input **and output devices**

...Abstract (Basic): The method of transferring blocks involves scheduling DMA block transfers based upon an availability of **data** from **several input** -output devices. An **input** -output **controller** (120) is coupled to a central processor (34) and **many input** -output devices (127, and 129). Each **input** -output device includes a buffer...
...The **controller** transfers **data** from the **input** -output **device** to a **memory** based upon availability of **data** in one of the buffers. **Data** blocks are **interleaved** on the basis of **locations** of scatter gather physical region descriptor entries in a table...

...ADVANTAGE - For multi-tasking data processing systems. Balanced, high aggregate system performance due to tuning **controller** . Improved input-output performance...
...Title Terms: **MEMORY** ;

34/3,K/19 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

010167310 **Image available**
WPI Acc No: 1995-068563/199510
XRPX Acc No: N95-054451
Shared cache for multiprocessor system - has local and shared cache using interleaving , multi-porting, pipelining and burst transfers to service each processor each cycle
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: DIBRINO M T; HICKS D A; LATTIMORE G M; SO K K; YOUSSEF H
Number of Countries: 005 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 637799	A2	19950208	EP 94304536	A	19940622	199510	B
US 5581734	A	19961203	US 93101144	A	19930802	199703	
EP 637799	A3	19970402	EP 94304536	A	19940622	199728	
JP 3360700	B2	20021224	JP 94140434	A	19940622	200304	

Priority Applications (No Type Date): US 93101144 A 19930802
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 637799	A2	E	16	G06F-012/08	
Designated States (Regional): DE FR GB					
US 5581734	A		14	G06F-012/08	
EP 637799	A3			G06F-012/08	
JP 3360700	B2		16	G06F-012/08	Previous Publ. patent JP 7056813

... **has local and shared cache using** interleaving , **multi-porting, pipelining and burst transfers to service each processor each cycle**

...Abstract (Basic): The multiprocessor system includes local and shared cache **memories** . A number of processors (3) each have their own local cache (L1) for rapid accesses. These caches communicate with system **memory** via a shared cache (100). The shared cache is controlled by a **memory** control unit (10...

...The shared cache is **interleaved** and uses pipelining on its read and **store** actions. Multiple ports are provided and allocation of ports to transactions is controlled on a least recently serviced priority basis by the **memory controller** . Burst mode transfers are held in **registers** to free the cache **memory** .
...

...ADVANTAGE - Provides service for each processor on each machine cycle and offers high performance **memory** .

...Abstract (Equivalent): A **data** processing system, having a **plurality** of processing units, comprising...

...units, in an amount greater than a capacity of said system bus, said circuit means **sequentially** storing said input data as data words, combining adjacent ones of said data words and...

...wherein said single operation simultaneously transfers said **data** between said cache and said **plurality** of processing units...
...Title Terms: **INTERLEAVED** ;

34/3,K/25 (Item 25 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009308723 **Image available**
WPI Acc No: 1993-002159/199301
XRPX Acc No: N93-001520
Direct access storage **device array for** storage **subsystems - uses array hierarchy which comprises number of RAID 3 arrays attached to common** controller **, to form RAID 5 array, providing high concurrency of RAID 5 array and high bandwidth of RAID 3 array**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: MENON J M; WOOD L C
Number of Countries: 004 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 521630	A2	19930107	EP 92305513	A	19920616	199301	B
US 5301297	A	19940405	US 91725696	A	19910703	199413	
EP 521630	A3	19940216	EP 92305513	A	19920616	199518	

Priority Applications (No Type Date): US 91725696 A 19910703
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 521630	A2	E	19	G06F-011/00	
Designated States (Regional): DE FR GB					
US 5301297	A		16	G06F-012/06	
EP 521630	A3			G06F-011/00	

Direct access storage **device array for** storage **subsystems**...

...**uses array hierarchy which comprises number of RAID 3 arrays attached to common** controller **, to form RAID 5 array, providing high concurrency of RAID 5 array and high bandwidth**...

...Abstract (Basic): A **storage** subsystem comprises a number of RAID 3 (Redundant Arrays of Inexpensive Discs) arrays of direct access **storage** devices (DASDs). Each RAID 3 **array** includes N **data** + P parity DASDs attached to a local **controller** .
...

...arrays to form a RAID 5 array of logical devices. The RAID 3 arrays are **addressable** through a path which includes the control unit and local **controllers** . The control unit receives data strings which are segmented into N blocks. The P parity
...Abstract (Equivalent): The method involves teaching insertion of **addressing** indirection to form and to access an array hierarchy expressly permitting the concurrency of a...

...a lower level RAID array, and after a DASD failure minimum spanning involvement when the **array** is rebuilding and rewriting missing **data** to a spare logical device...

...Also, disclosed are the accessing of variable length **records** on the array hierarchy, array hierarchy in which RAID 5 arrays have dissimilar number of logic devices (lower level RAID arrays) and **interleave** depths. Logical arrays are formed using fractional **storage** defined onto real DASD subsets. Logical devices are defined onto DASDs distributed in the same...
...Title Terms: **STORAGE** ;

34/3,K/29 (Item 29 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008562987 **Image available**
WPI Acc No: 1991-067022/199110
XRPX Acc No: N91-051865
Main memory **control system for computer - has initial data generating initialisation control and refresh control circuits**
Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)
Inventor: HIROSAWA T
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 415433	A	19910306	EP 90116715	A	19900831	199110	B
CA 2024433	A	19910302				199131	
US 5235691	A	19930810	US 90575960	A	19900831	199333	
CA 2024433	C	19940208	CA 2024433	A	19900831	199411	
EP 415433	B1	19950412	EP 90116715	A	19900831	199519	
DE 69018542	E	19950518	DE 618542	A	19900831	199525	
			EP 90116715	A	19900831		

Priority Applications (No Type Date): JP 89224522 A 19890901
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 415433	A				
Designated States (Regional): DE FR GB					
US 5235691	A		10	G06F-012/16	
EP 415433	B1	E	15	G11C-011/406	
Designated States (Regional): DE FR GB					
DE 69018542	E			G11C-011/406	Based on patent EP 415433
CA 2024433	C			G06F-009/30	

Main memory **control system for computer**...

...Abstract (Basic): A main **memory** control system has an initial **data** generating circuit for generating initial data, an initialisation control circuit for activating an initialise signal...

...When the initialise signal is inactive, the main **memory** control system performs normal read, **write** , and refresh operations. When the initialise signal is active, the main **memory** control system selects the initial **data** by means of a **data** **multiplexer** and performs only **write** operati6ns, **writing** the initial **data** at refresh **addresses** generated by the refresh control circuit. If the main **memory** has an **interleaved** structure, the initial **data** are written in all leaves simultaneously...

...USE/ADVANTAGE - Initialising main **memory** of computer rapidly, using only simple additional hardware. Can initialise all leaves of **interleaved** main **memory** simultaneously. (11pp Dwg.No.1/4)
...Abstract (Equivalent): A main **memory** control system for controlling access to a main **memory** of a computer by a central processing unit of the computer, and for refreshing and initializing the main **memory** , comprising: an initial **data** generating means for generating initial data; an initialization control means connected to said central processing...

...response thereto; a refresh control means connected to said initialization control means, for generating refresh **addresses** and

activating a refresh timing signal; a **memory** control means connected to said refresh control means, said initial data generating means said initialization control means, said main **memory** , and said central processing unit for selecting said refresh addresses when said refresh timing signal...

...central processing unit when said initialize signal is inactive and for generating control signals for **writing** the selected **data** at the selected **addresses** in said main **memory** ; characterised in that said refresh timing signal is activated at selectable refresh intervals, and said...

...Abstract (Equivalent): A main **memory** control system has as initial **data** generating circuit for generating initial data, an initialisation control circuit for activating an initialise signal...

...When the initialise signal is inactive, the main **memory** control system performs normal read, **write** , and refresh operations. When the initialise signal is active, the main **memory** control system selects the initial **data** by means of a **data** **multiplexer** and performs only **write** operations, **writing** the initial **data** at refresh **addresses** generated by the refresh control circuit. If the main **memory** has an **interleaved** structure, the initial **data** are written in all banks simultaneously...

...USE/ADVANTAGE - For controlling main **memory** of a computer, particularly system with means of initialising main **memory** , using only simple additional hardwork. Scrubbing refresh, RAS-only refresh or CAS - before - RAS refresh...

...Title Terms: **MEMORY** ;

34/3,K/34 (Item 34 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004605246
WPI Acc No: 1986-108590/198617
XRPX Acc No: N86-080027
Dynamically allocated local-global storage **system - for multi-processor system by assigning first and second** storage **portions to reference and any other processor respectively**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: BRANTLEY W C; MCAULIFEE K P; NORTON V A; PFISTER G F; WEISS J
Number of Countries: 007 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
GB 2165975	A	19860423	GB 8525903	A	19851021	198617 B
EP 179401	A	19860430	EP 85113174	A	19851017	198618
CA 1236588	A	19880510				198823
CN 8507534	A	19870415				198827
US 4754394	A	19880628	US 84664131	A	19841024	198828
GB 2165975	B	19880720				198829
US 4980822	A	19901225	US 88168721	A	19880316	199103
EP 179401	B1	19920722	EP 85113174	A	19851017	199230
DE 3586389	G	19920827	DE 3586389	A	19851017	199236
			EP 85113174	A	19851017	

Priority Applications (No Type Date): US 84664131 A 19841024; US 88168721 A 19880316
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2165975	A		12		
EP 179401	A	E			
Designated States (Regional): DE FR GB IT					
EP 179401	B1	E		G06F-012/02	
Designated States (Regional): DE FR GB IT					
DE 3586389	G			G06F-012/02	Based on patent EP 179401

Dynamically allocated local-global storage **system**...

...**for multi-processor system by assigning first and second** storage **portions to reference and any other processor respectively**

...Abstract (Basic): A table look-up provides a quantity, the **interleave** amount, which indicates whether the real **address** is in local or global **storage** and, which in the latter event, is used to derive the absolute **addresses** . The low order bits of the real **address** may be hashed using Remap (252) to introduce a random element into a **sequence** of consecutive **addresses** . The rear **address** after mapping excluding the word offset (WO) is passed to right rotate device (256) which is controlled by the **interleave** amount...

...be rotated and the amount the field is to be rotated are specified by the **interleave** amount. The derived absolute **addresses** are entered in **register** (258) and are passed for use onto a communication network interconnecting the processors and the **storage** system. Local and global **storage** is distributed amongst the nodes of a multiprocessor network. (12pp Dwg.No.7/8)
...Abstract (Equivalent): **Data** processing apparatus comprising a communications network having **plural** individually **addressable** ports with a processor and a **storage** unit connected to at least some, and

potentially all, of the ports providing **addressable** processing nodes, the network being arranged to support node **address** containing message passing from any originating processing node and the **addressed** node, each processor incorporating a table driven, virtual to real **address** translation facility and an interface mechanism, in part controlled thereby, providing bi-directional communication between the processor, its connected port and the local **storage** unit, the translation facility responding to a virtual **address** from the processor to derive a processing node **address** which, if it is the local processing node **address** , causes the interface to connect the processor and the local **storage** unit and, if it is not the local processing node **address** , to connect the processor and the network via the local port and a message cotnaining the generated other node **address** , and hence, indirectly, to the **addressed** processing node, the interface mechanism at the **addressed** processing node connecting the port to the **storage** unit local to that port, the translation control tables being writable at run time to match the requirements of applications, whereby the real **address** space of any particular processor is variably divided between its local **storage** unit and global **storage** in the form of the aggregate of the **storage** units in other processing nodes, and the local **storage** unit is equally variably divided between local **storage** and global **storage** , directly by the translation defined by the local translation control tables.

...Abstract (Equivalent): The method comprises the steps of mapping virtual **addresses** of **storage** reference requests produced by processors to real **addresses** , each of the real **addresses** having high-order bits for **identifying** one of the **memory** modules in one of the processing nodes and low-order bits for **identifying** a **storage location** in the **identified memory** module and selectively swapping a variable number of the high-order bits for the same number of the low-order bits of the real **addresses** to generate corresponding absolute **addresses** .

...

...of said high-order bits and low-order bits to be swapped and directing the **storage** reference requests from each processor in accordance with the absolute **addresses** to either the **memory** module in its respective processing nodeor to other **memory** modules in remote processing nodes via the communication network...

...The multiprocessing system includes a map/ **interleave** block for applying variable **interleaving** transformation to the real **addresses** of the **storage** reference requests produced by the processor, the real **addresses** transforming to corresp. absolute **addresses** with each absolute **address** **identifying** one of the **memory** modules and a **storage location** . A **controller** , under the dynamic control of the processor responding to the user software during run time operates on the map/ **interleave** block to **interleave** the absolute **addresses** across varying numbers of **memory** modules...

...A device coupled to the map/ **interleave** block directs **storage** reference requests in accordance with the absolute **addresses** to the respective **identified** **memory** modules and **locations** . Blocks of absolute **addresses** are dynamically **interleaved** across variable numbers of the **memory** modules as specified by the **controller** .

...

...ADVANTAGE - Allows **storage** configuration to be dynamically altered to fit needs of user and improves performance over wide

...Title Terms: **STORAGE** ;

34/3,K/38 (Item 38 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003309553
WPI Acc No: 1982-F7562E/198220
Memory controller **appts. for processing number of** memory **requests - has** several **queue circuits having** address , **control and** data **queue** registers **and tri-state flip-flop for independent operation**
Patent Assignee: HONEYWELL INFORM SYSTEMS INC (HONE)
Inventor: JOHNSON R B; NIBBY C M
Number of Countries: 014 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 51426	A	19820512				198220	B
FI 8103266	A	19820630				198229	
BR 8106954	A	19820713				198230	
US 4451880	A	19840529	US 80202821	A	19801031	198424	
CA 1172771	A	19840814				198437	
KR 8600986	B	19860724				198650	

Priority Applications (No Type Date): US 80202821 A 19801031
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 51426	A	E	107		

Designated States (Regional): BE CH DE FR GB IT LI NL SE

Memory controller **appts. for processing number of** memory **requests** ...

...**has** several **queue circuits having** address , **control and** data **queue** registers **and tri-state flip-flop for independent operation**

...Abstract (Basic): The **controller** has at least 2 queue circuits for storing **memory** requests. A queue control circuitry **sequentially** enables the queue circuits for processing the **memory** requests from units coupled to a bus connected to the **controller** . Each queue circuit has a first **register** for storing the **addresses** of the **memory** requests. A second **register stores** the type of **memory** requests and a third **register stores** the data of **memory** requests if they are of the **write** type...

...Each queue circuit also has a bistable request indicator which is set on a **memory** request being **stored** to inhibit further storing of requests in that queue circuit. Each **address** queue **register** has a tristate flip-flop for enabling independent operation in processing **memory** requests. The flip-flop is controlled by an Exclusive-OR circuit having one input energised by a predetermined state of the flip-flop. The **controller** enables **interleaving** of **memory** requests, eliminating processing delays.
...Abstract (Equivalent): The **controller** controls the operation of a number of **memory** module units and includes a number of queues which couple to the module units. Each queue includes an **address** queue **register** , a control queue **register** and a data queue **register** . Each **address** queue **register** has tristate control for independent operation...

...Control circuits which couple to the queue **address** , control and data **registers** assign **memory** cycles between queues on an alternate basis when the queue control **registers store** requests which are being

processed. This enables the **interleaving** of **memory** requests which eliminates processing delays particularly in cases where such requests involve multi word transfers over successively **memory** cycles of operation.

Title Terms: **MEMORY** ;

34/3,K/39 (Item 39 from file: 347)
DIALOG(R)File 347:JAPIO

06446472 **Image available**
DATA MULTIPLEXER , DATA MULTIPLEXING METHOD, AND COMPUTER READABLE **RECORDING** MEDIUM **RECORDED** WITH THE **DATA MULTIPLEXING** METHOD

PUB. NO.: 2000-032042 [JP 2000032042 A]
PUBLISHED: January 28, 2000 (20000128)
INVENTOR(s): TOMOTA MASAAKI
SATO KENSUKE
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD
APPL. NO.: 10-192889 [JP 98192889]
FILED: July 08, 1998 (19980708)

DATA MULTIPLEXER , DATA MULTIPLEXING METHOD, AND COMPUTER READABLE **RECORDING** MEDIUM **RECORDED** WITH THE **DATA MULTIPLEXING** METHOD

ABSTRACT

PROBLEM TO BE SOLVED: To **interleave plurality** of **input** fixed length **packet** streams efficiently.

SOLUTION: A **multiplex** request generating sections 101-103 calculate a time when a **packet** stream is **multiplexed** based on an output rate of an output fixed length packet stream and an input rate of an **input** fixed length **packet** stream and outputs a **multiplex** request when the time reaches an output reference time by an output reference time management **section** 107. Queue **sections** 104-106 **store** temporarily respective multiplex requests outputted from the multiplex request generating sections. A selection signal generating...

...according to a prescribed retrieval sequence and provides an output of a selection signal. An **interleave section** 109 **interleaves** the **packet** stream according to the selection signal. Thus, invalid **packets** detected by an invalid **packet** delete **section** are deleted and **interleaving** with other **input packet** stream is attained and the packing rate of the **packet** stream is enhanced.

```
Set      Items   Description
S1       11699   (EXTEND? OR EXTRA? OR REDUND? OR SECOND? OR 2ND OR BACKUP?
             OR BACK?()UP)(2N)(REMOTE? OR OFFSITE? OR DISTAL? OR DISTANT? -
             OR GLOBAL? OR ("NOT" OR NON)()LOCAL? OR OFF()SITE)
S2     2523704   COPY? OR STORE? OR STORAGE? OR WRITE? OR WRITING?
S3     2173310   RECORD? OR MEMOR? OR BACKUP? OR BACK?()UP
S4      160968   (MAGNETIC OR MEMOR?)(2N)(STORAG? OR TAPE? OR DEVIC? OR DIS-
             K? OR DISC?)
S5      736683   CONTROLLER? OR MANAGER? OR SUPERVISOR? OR AUTHORIT?
S6        2417   (STORAG? OR DATA?)()(MOVER? OR ROUTER? OR MULTIPLEX? OR MU-
             X?)
S7     7260327   MULTIP? OR MULTIT? OR PLURAL? OR MANY? OR SEVERAL? OR ARRA-
             Y? OR MULTITHREAD? OR MULTI()THREAD? OR RAID
S8    12173252   DATA? OR PACKET? OR INPUT? OR THREAD? OR INFORMATION? OR I-
             NFO? OR FILE? OR SOURC?
S9      104458   INTERMINGL? OR INTERMIX? OR INTERLEAV? OR COALESC?
S10      24270   COMMINGL? OR COMMIX? OR INTERLAC? OR SHUFFL? OR INTERWEAV?
S11    1655517   CHRONICL? OR ARCHIV? OR LOG OR LOGS OR LOGGED OR LOGGING? -
             OR INDEX?
S12    3262402   HISTOR? OR TRACK? OR LIBRAR? OR RECORD? ? OR DIARY? OR REG-
             IST? OR LIST? ?
S13    2860810   MONITOR? OR WATCH? OR AUDIT? OR ACCOUNT?
S14   10200220   LOCATION? OR ADDRESS? OR SITE? ? OR LOCALE? OR POSITION? OR
             SECTOR? OR LOCUS? OR SECTION? OR SEQUEN? OR IDENTIF?
S15     233190   *deleted*  S2:S4(7N)S7(7N)S7
S16      44839   S2:S4(7N)S7(7N)S8
S17         61   S16 AND S1
S18       3735   S16:S17 AND S9:S11
S19          6   S17 AND S18
S20        470   S16:S17 AND S9:S10
S21          0   S20 AND S17
S22         45   S20 AND S11:S13 AND S14
S23         51   S19 OR S22
S24         46   S23 AND PY<2004
S25         33   RD (unique items)
S26         25   S1:S4 AND S5:S6 AND S7 AND S8 AND S9:S10 AND S11:S13 AND S-
               14
S27         24   S26 AND PY<2004
S28         18   RD (unique items)
File   2:INSPEC 1969-2005/Sep W3
         (c) 2005 Institution of Electrical Engineers
File   6:NTIS 1964-2005/Sep W3
         (c) 2005 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2005/Sep W3
         (c) 2005 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2005/Sep W3
         (c) 2005 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2005/Aug
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File  65:Inside Conferences 1993-2005/Sep W4
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File  94:JICST-EPlus 1985-2005/Jul W5
         (c)2005 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2005/Jul
         (c) 2005 The HW Wilson Co.
File 111:TGG Natl.Newspaper Index(SM) 1979-2005/Sep 22
         (c) 2005 The Gale Group
File 144:Pascal 1973-2005/Sep W3
         (c) 2005 INIST/CNRS
File 239:Mathsci 1940-2005/Nov
         (c) 2005 American Mathematical Society
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Biblio 6 Files

File 256:TecInfoSource 82-2005/Sep
(c) 2005 Info.Sources Inc

25/3,K/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

05838420 INSPEC Abstract Number: C9501-5440-013
Title: Interleaved **parallel schemes**
Author(s): Seznec, A.; Lenfant, J.
Author Affiliation: IRISA, Rennes, France
Journal: IEEE Transactions on Parallel and Distributed Systems vol.5, no.12 p.1329-34
Publication Date: Dec. 1994 Country of Publication: USA
CODEN: ITDSEO ISSN: 1045-9219
U.S. Copyright Clearance Center Code: 1045-9219/94/$04.00
Language: English
Subfile: C

Title: Interleaved **parallel schemes**
Abstract: On vector supercomputers, vector **register** processors share a global highly **interleaved** **memory** . In order to optimize **memory** throughput, a single-instruction, **multiple - data** (SIMD) synchronization mode may be used on vector **sections** . We present an **interleaved** parallel scheme (IPS). Using IPS ensures an equitable distribution of elements on a highly **interleaved** memory for a wide range of vector strides. Access to memory may be organized in...
Identifiers: **interleaved** parallel schemes...

...vector **register** processors...

...global highly **interleaved** memory...
1994

25/3,K/13 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1757453 NTIS Accession Number: N93-30464/0
Striped Tertiary Storage Arrays
Drapeau, A. L.
California Univ., Berkeley.
Corp. Source Codes: 005029000; CC747787
Sponsor: National Aeronautics and Space Administration, Washington, DC.
1993 11p
Languages: English
Journal Announcement: GRAI9323; STAR3111
In NASA. Goddard Space Flight Center, Goddard Conference on Mass Storage Systems and Technologies, Volume 1, p 203-213.
NTIS Prices: (Order as N93-30449/1, PC A15/MF A03)

...technique for increasing the throughput and reducing the response time of large access to a **storage** system. In striped **magnetic** or optical **disk arrays**, a single **file** is striped or **interleaved** across **several** disks; in a striped tape system, **files** are **interleaved** across tape cartridges. Because a striped **file** can be accessed by **several** disk drives or tape **recorders** in parallel, the sustained bandwidth to the **file** is greater than in non-striped systems, where access to the file are restricted to...
... using large tertiary storage systems is discussed. It will introduce commonly available tape drives and **libraries**, and discuss their performance limitations, especially focusing on the long latency of tape accesses. This **section** will also describe an event-driven tertiary storage array simulator that is being used to...

...are discussed, and plans for modeling the overall reliability of striped tertiary storage arrays to **identify** the amount of error correction required are described. Finally, work being done by other members of the Sequoia group to **address** latency of accesses, optimizing tertiary storage arrays that perform mostly writes, and compression is discussed.

25/3,K/25 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01851839 ORDER NO: AADAA-I3025179
Algorithms and methodology for scalable model checking
Author: Qadeer, Shaz
Degree: Ph.D.
Year: **1999**
Corporate Source/Institution: University of California, Berkeley (0028)
Source: VOLUME 62/09-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 4148. 150 PAGES
ISBN: 0-493-36991-0

Year: **1999**

...variables and □30K gates.
Our third contribution is a systematic model checking methodology for **multiprocessor** systems with three parameters—number of processors, number of **memory locations** , and number of **data** values. **Sequential** consistency requires that some **interleaving** of the local temporal orders of read/write events at different processors be a trace of serial memory. Therefore, it suffices to construct a non-interfering serializer that **watches** and reorders read/write events so that a trace of serial memory is obtained. While...
...such a serializer must be unbounded even for fixed values of the parameters—checking **sequential** consistency is undecidable!—we show that the paradigmatic class of snoopy cache coherence protocols...

...of processors and use the notion of a serializer to reduce the problem of verifying **sequential** consistency to that of checking language inclusion between finite state machines.

25/3,K/28 (Item 4 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01243804 ORDER NO: AAD92-30248
DISASTER RECOVERY FOR TRANSACTION PROCESSING SYSTEMS
Author: POLYZOIS, CHRISTOS A.
Degree: PH.D.
Year: **1992**
Corporate Source/Institution: PRINCETON UNIVERSITY (0181)
Source: VOLUME 53/06-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 2991. 109 PAGES

Year: **1992**

A **remote backup** is a copy of a primary database maintained at a geographically separate location and is used to increase data availability. **Remote backup** systems are usually **log** -based and can be classified as either 2-safe or 1-safe, depending on whether...

...sites simultaneously or they commit first at the primary and are then propagated to the **backup** .

This thesis describes 1-safe algorithms that can exploit **multiple log** streams to propagate **information** from the primary to the **backup** . An experimental distributed **database** system is used to evaluate the performance of these algorithms and compare the 1-safe...

28/3,K/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

03338441 INSPEC Abstract Number: C84050627
Title: Analysis of interleaved storage **via a constant-service queuing system with Markov-chain-driven** input
Author(s): Hofri, M.
Author Affiliation: Technion-Israel Inst. of Technol., Haifa, Israel
Journal: Journal of the Association for Computing Machinery vol.31, no.3 p.628-48
Publication Date: July 1984 Country of Publication: USA
CODEN: JACOAH ISSN: 0004-5411
U.S. Copyright Clearance Center Code: 0004-5411/84/0700-0628$00.75
Language: English
Subfile: C

Title: Analysis of interleaved storage **via a constant-service queuing system with Markov-chain-driven** input
Abstract: A popular means of increasing the effective rate of main **storage** accesses in a large computer is a **multiplicity** of **memory** modules accessible in parallel. Although such an organization usually achieves a net gain in access rate, it also creates new modes of congestion at the **storage controller** . This paper analyzes the variables that describe such a congestion: queue lengths and delays. A **controller** that maintains separate **register** sets to accommodate the request queue of each module is considered. The various processors attached to the **storage** are assumed to generate, in each **memory** cycle, a number of access requests with the same given distribution. The **addresses** specified by these requests (reduced to the module **index**) are further assumed to follow the states of a first-order Markov chain. The analysis then becomes one of a single-server queuing system with constant service time and **indexed** batch arrival process. Results are derived for **several** descriptors of the congestion and thus of the quality of service offered by such an...
Descriptors: **data** handling...

... **file** organisation
Identifiers: **interleaved storage** ; ...

...Markov-chain-driven **input** ; ...

... **memory** modules...

... storage controller
1984